

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 1. (Original) A method of transferring bursts of data between
2 a processor device and a FIFO device, said transfer comprising:
3 triggering a burst transfer from the change of state of a FIFO
4 output signal, said change of state being the occurrence of a
5 triggering event within the FIFO device; and
6 inhibiting of triggering of any further burst transfers until
7 a current burst transfer is complete.

1 2. (Original) The method of claim 1, wherein:
2 said triggering event is change in a FIFO fullness indicator
3 flag.

1 3. (Original) The method of claim 2, wherein:
2 said FIFO fullness indicator flag denotes the FIFO is less
3 than or greater than half full; and
4 said triggering event is changing from said FIFO fullness
5 indicator flag denoting less than half full to greater than half
6 full.

1 4. (Original) The method of claim 2, wherein:
2 said fullness indicator denotes less than or greater than half
3 full; and
4 said triggering event is changing from said FIFO fullness
5 indicator flag denoting greater than half full to less than half
6 full.

1 5. (Original) The method of claim 1, wherein:
2 said burst transfer includes transfer of predetermined amount
3 of data in fixed number of sequential clock cycles.

1 6. (Currently Amended) The method of claim 5, wherein:
2 said predetermined amount of data in a the burst transfer is
3 set by an input to the FIFO device from the processor device during
4 initialization.

1 7. (Original) The method of claim 5, wherein:
2 said predetermined amount of data in a burst transfer is set
3 by an input to a programmable FIFO device register.

1 8. (Currently Amended) The method of claim 7, wherein:
2 the processor device supplies aid said predetermined amount of
3 data to said programmable FIFO device register via an output pin.

1 9. (Original) The method of claim 1, further comprising the
2 step of:
3 inhibiting trigger from processor device, thereby inhibiting
4 further burst transfers until a predetermined number of clock
5 cycles following completion of current burst transfer.